Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claim 1 (Currently Amended): A method of fabricating a semiconductor device comprising:

providing a support substrate;

forming, on [[a]] the support substrate, through an oxide film, an SOI layer that has an element formation region and an element isolation region;

[[ion]] implanting an impurity to the support substrate through the SOI layer in the neighborhood of ~~the oxide film~~ a boundary between the element formation region and the element isolation region so as to form a low electric resistance layer on the support substrate that extends ~~extend~~ from a lower portion of the element formation region to a lower portion of the element isolation region ~~and thereby making the support substrate of a portion where the impurity is ion implanted a low electric resistance layer~~;

heating the support substrate;

forming an element isolation layer in the element isolation region of the SOI layer; and

forming a contact that penetrates through the element isolation layer and the oxide film in the neighborhood of the boundary between the element formation region and the element isolation region to reach the low electric resistance layer.

Claim 2 (Original): A method of fabricating a semiconductor device as set forth in claim 1:

wherein the contact has an adherence layer in a portion that comes into contact with the support substrate.

Claim 3 (Original): A method of fabricating a semiconductor device as set forth in claim 1:

wherein the impurity is As.

Claim 4 (Original): A method of fabricating a semiconductor device as set forth in claim 1 further comprising:

forming a semiconductor element having a diffusion layer in the element formation region of the SOI layer;

wherein heat treatment of the diffusion layer and heat treatment of the support substrate are simultaneously applied.

Claim 5 (Original): A method of fabricating a semiconductor device as set forth in claim 1 further comprising:

forming an element isolation layer in the element isolation region of the SOI layer by use of heat treatment;

wherein heat treatment of the element isolation layer and heat treatment of the support substrate are simultaneously applied.

Claims 6-8 (Canceled)

Claim 9 (New): A method of manufacturing a semiconductor device, comprising:

providing an SOI substrate having an element formation region and an isolation region, the SOI substrate including a semiconductor substrate, a buried insulating layer formed on the semiconductor substrate and an SOI layer formed on the buried insulating layer;

introducing an impurity into the semiconductor substrate around a boundary between the element formation region and the isolation region through the buried insulating layer and the SOI layer so that an impurity region extending from the element formation region to the isolation region is formed on the semiconductor substrate;

subjecting the SOI substrate to a heat treatment;

forming an isolation layer in the isolation region so that the SOI layer in the element formation region is surrounded by the isolation layer;

forming a through hole in the isolation region near the element formation region through the isolation layer and the buried insulating layer so that the through hole exposes the impurity region; and

filling a conductive material into the through hole.

Claim 10 (New): A method of manufacturing a semiconductor device according to claim 9, wherein said introducing includes implanting impurity ions into the semiconductor substrate.

Claim 11 (New): A method of manufacturing a semiconductor device according to claim 9, wherein the impurity is As.

Claim 12 (New): A method of manufacturing a semiconductor device according to claim 9, wherein the isolation layer is formed by a LOCOS method.

Claim 13 (New): A method of manufacturing a semiconductor device according to claim 9, wherein the conductive material includes an adhesion layer made of TiN formed on the impurity region and a plug formed on the adhesion layer.

Claim 14. (New) A method of manufacturing a semiconductor device according to claim 13, wherein the plug is made of W.

Claim 15 (New): A method of manufacturing a semiconductor device according to claim 13, wherein the plug is made of polysilicon.

Claim 16 (New): A method of manufacturing a semiconductor device, comprising:

providing an SOI substrate having an element formation region and an isolation region, the SOI substrate including a semiconductor substrate, a buried oxide layer formed on the semiconductor substrate and an SOI layer formed on the buried oxide layer;

introducing ions into the semiconductor substrate in an area including a boundary between the element formation region and the isolation region through the

buried oxide layer and the SOI layer so as to form a low resistive layer extending from the element formation region to the isolation region on the semiconductor substrate;

subjecting the SOI substrate to a heat treatment;

forming an isolation layer in the isolation region so that the SOI layer in the element formation region is surrounded by the isolation layer;

forming a contact hole in the isolation region within an area through the isolation layer and the buried oxide layer so that the contact hole exposes the low resistive layer; and

filling a conductive material into the contact hole.

Claim 17 (New): A method of manufacturing a semiconductor device according to claim 16, wherein said introducing includes implanting As ions into the semiconductor substrate.

Claim 18 (New): A method of manufacturing a semiconductor device according to claim 16, wherein the isolation layer is formed by a LOCOS method.

Claim 19 (New): A method of manufacturing a semiconductor device according to claim 16, wherein the conductive material includes an adhesion layer made of TiN formed on the low resistive layer and a plug formed on the adhesion layer.

Claim 20 (New): A method of manufacturing a semiconductor device according to claim 19, wherein the plug is made of W.

Claim 21 (New): A method of manufacturing a semiconductor device according to claim 19, wherein the plug is made of doped polysilicon.